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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/683,858	10/10/2003	Vladislav Vashchenko	P05701	1770
7590	07/08/2004		EXAMINER	
Jurgen Vollrath 588 Sutter Street #531 San Francisco, CA 94102			LUHRS, MICHAEL K	
			ART UNIT	PAPER NUMBER
			2824	

DATE MAILED: 07/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/683,858	VASHCHENKO ET AL. <i>(initials)</i>	
	Examiner Michael K. Luhrs	Art Unit 2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 10 October 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-18 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 10 October 2003 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input checked="" type="checkbox"/> Other: <u>search history</u> . |

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 8 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: the formation of the snap back devices. Applicant claims annealing (claim 8) and exposing to temperature (claim 9) of the 'snap back devices', yet has only provided the single step of using a mask of varying degrees of perforation during formation of 'isolation layers'.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6 and 10-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Taft et. al.

USPN 5,300,454.

Regarding independent claim 1, Taft et. al. teach using a perforated mask during doping of the doped region, the mask having a predefined ratio of perforation to mask material, as mask '14' (lines 44-45, column 2) having rectangular openings defined (lines 55-56, column 2) or checkerboard (lines 56-57, column 3) is thus perforated, and doping occurs (in lines 62-63, column 2) through the openings to form doped regions '16' (line 64, column 2).

Regarding claim 2, Taft et. al. teach comprising annealing the doped region, in lines 67-68, column 2, as thermal cycle or heating step.

Regarding claim 3, Taft et. al. teach further comprising exposing the doped region to one or more predefined elevated temperatures for predefined times, in lines 67-68, column 2, as thermal cycle or heating step.

Regarding independent claim 4, Taft et. al. teach providing a perforated mask (as discussed above for claim 1-- please refer back), with varying ratios of masked portion to unmasked portion, as shown by Fig. 6 having a ratio of openings i.e. 'Y' masked to 'X' unmasked' and varies as seen in Fig. 6 region of unmasked area '22', i.e. the unmasked area is more, would thus be a mask having a varying ratio, i.e. not just one ratio, and applying dopant to the IC to define doped regions, as the dopant applied in Fig. 5, (line 31, column 3) for a twin well (line 48, column 3) comprised IC.

Regarding claim 5, Taft et. al. teach comprising annealing the doped region, as discussed previously above for claim 2: Taft et. al. teach comprising annealing the doped region, in lines 67-68, column 2, as thermal cycle or heating step.

Regarding claim 6, Taft et. al. teach comprising exposing the doped region to one or more predefined elevated temperatures for predefined times in lines 67-68, column 2, as thermal cycle or heating step.

Regarding independent claim 10, Taft et. al. teach controlling doping levels of an isolation region by using a perforated mask as discussed in lines 39-44, column 4--that the mask can control the doping concentration and junction depth for a device, and for example a well region '42' can be formed using a mask having multiple openings, (lines 44-49, column 4) of Fig. 2 or Fig 8, i.e. Fig. 8 is perforated, during doping of the isolation region, i.e. any of the doping lines 62-64, column 2 through column 5, specifically doping described in lines 63-66 column 5 or buried layers line 1, column 6, or for doping profile and concentration in SIMOX or nitrogen (lines 40-46, column 6).

Regarding claim 11, Taft et. al. teach further comprising annealing the device in lines 67-68, column 2, as thermal cycle or heating step, see also as thermal cycle (line 29, column 5).

Regarding claim 12, Taft et. al. teach comprising exposing the doped region to one or more predefined elevated temperatures for predefined times in lines 67-68, column 2, as thermal cycle or heating step, see also as thermal cycle (line 29, column 5).

Regarding independent claim 13, Taft et. al. teach forming an isolation layer between active regions and substrate of the device, wherein the isolation layer includes forming spotted implants, as

Regarding claim 14, Taft et. al. teach wherein the spotted implants are formed by making use of a mask with intermittent openings, as two or more doped regions '24' and '26' using the inventive mask (line 67, column 5) having openings previously discussed above.

Regarding claim 15, Taft et. al. wherein the spotted implants are provided before one or both of an epitaxial layer being grown and high diffusion drive taking place, as epitaxial growth layer '100' (line 9, column 6, after, i.e. 'once doped regions have been formed' (line 5, column 6).

Regarding claim 16, Taft et. al. teach, wherein the snapback device is an ESD protection device, as any of "BiCMOS, microcontroller circuits, combined digital/analog circuits, memory arrays and the like" (lines 33-35, column 6), inherently, as any of the doped regions formed in microcontroller circuitry having inclusive thereto ESD protective devices having the doped implant provided thereto.

Regarding claim 17, Taft et. al. teach further comprising annealing the device, as discussed previously above for claims 5 and 11: again, see lines 67-68, column 2, as thermal cycle or heating step, and see also as thermal cycle (line 29, column 5).

Regarding claim 18, Taft et. al. teach, further comprising exposing the device to one or more predefined elevated temperatures for predefined times, as discussed previously above for claims 6 and 12: again, see lines 67-68, column 2, as thermal cycle or heating step, and see also as thermal cycle (line 29, column 5).

5. Claims 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Ahn et. al. USPN 5,567,645.

Regarding independent claim 7, Ahn et. al. teach using a mask of varying degrees of perforation during formation of the isolation layers, as shown in Fig. 1, isolation regions '5' and '6' masked by layer '2' having different widths w1 and w2, i.e. layer '2' is etched (line 37-38, column 1) is the mask for forming the isolation region (lines 38-41, column 1).

Regarding claim 8, Taft et. al. teach annealing in line 12, column 4.

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Regarding claim 9, Taft et. al. teach exposing to one or more predefined elevated temperatures for predefined times, as annealing in line 12, column 4.

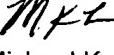
Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. ESD circuitry is expressed in USPN 5,869,366 and USPN 6,586,317.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael K. Luhrs whose telephone number is 571-272-1874. The examiner can normally be reached on M-F, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Michael K. Luhrs



ANH PHUNG
PRIMARY EXAMINER